the memory region including a split-gate non-volatile memory transistor,

the first transistor region including a first voltage-type transistor that operates at a first voltage level,

the second transistor region including a second voltage-type transistor that operates at a second voltage level, and

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the third transistor region including a third voltage-type transistor that operates at a third voltage level that is higher than the first and second voltage levels,

Concl'd

wherein the device includes a first thermally oxidized gate dielectric layer formed in the second transistor region, and

wherein the device includes a second thermally oxidized gate dielectric layer formed in the first transistor region and the second transistor region, wherein the second thermally oxidized gate dielectric layer in the second transistor region is positioned on the first thermally oxidized gate dielectric layer.

2. (amended) A semiconductor device according to claim 1, wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, and wherein the second thermally oxidized gate dielectric layer is also formed in the third transistor region as one of the at least three insulation layers.

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4. (amended) A semiconductor device according to claim 3, wherein the second outermost layer that contacts the control gate is formed in the same step in which the second thermally oxidized gate dielectric layer is formed.

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6. (amended) A semiconductor device according to claim 5, the third voltage-type transistor has a gate insulation layer formed from three insulation layers, and the gate insulation layer of the third voltage-type transistor has an identical thickness as the intermediate insulation layer of the non-volatile memory transistor.

7. (amended) A semiconductor device according to claim 6, wherein the first voltage-type transistor has a gate insulation layer formed from the second thermally oxidized layer and has a thickness of 3 – 13 nm.

8. (amended) A semiconductor device according to claim 7, wherein the second voltage-type transistor has a gate insulation layer that includes the first thermally oxidized layer and the second thermally oxidized layer and has a thickness of 4 – 15 nm.

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9. (amended) A semiconductor device according to claim 8, wherein the third voltage-type transistor has a gate insulation layer that includes the second thermally oxidized layer and at least two additional layers and has a thickness of 16 – 45 nm.

Concl'd

10. (amended) A semiconductor device according to claim 9, wherein the second thermally oxidized gate dielectric layer is also formed in the memory region, wherein the non-volatile memory transistor has an intermediate insulation layer that includes the second thermally oxidized layer.

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12. (amended) A semiconductor device comprising a memory region and first, second and third transistor regions including field effect transistors that operate at different voltage levels;

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the memory region including a split-gate non-volatile memory transistor,

the first transistor region including a first voltage-type transistor that operates at a first voltage level;

the second transistor region including a second voltage-type transistor that operates at a second voltage level; and

the third transistor region including a third voltage-type transistor that operates at a third voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed; and

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wherein the first voltage level that operates the first voltage-type transistor is 1.8 – 3.3 V, the second voltage level that operates the second voltage-type transistor is 2.5 – 5 V, and the third voltage level that operates the third voltage-type transistor is 10 – 15 V.

19. (amended) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

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a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the non-volatile memory transistor intermediate insulation layer has a thickness that is identical to that of the gate insulation layer of the third voltage-type transistor.

22. (amended) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

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a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers; and

wherein the first voltage level is in the range of 1.8 to 3.3 V, the second voltage level is in the range of 2.5 to 5 V, and the third voltage level is in the range of 10 to 15 V.

24. (amended) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

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wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate; and

wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, wherein the at least three insulation layers of the third voltage type transistor are identical in composition to the at least three insulation layers of the intermediate insulation layer of the non-volatile memory transistor.

26. (amended) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

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a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate;

wherein the first voltage-type transistor has a gate insulation layer having a thickness that is less than that of the second voltage-type transistor, and the second voltage-type transistor has a gate insulation layer having a thickness that is less than that of the third voltage type transistor; and

wherein the non-volatile memory transistor intermediate insulation layer has a thickness that is identical to that of the gate insulation layer of the third voltage-type transistor.

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27. (amended) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate;

wherein the first voltage-type transistor has a gate insulation layer having a thickness that is less than that of the second voltage-type transistor, and the second voltage-type transistor has a gate insulation layer having a thickness that is less than that of the third voltage type transistor;

and

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wherein the first voltage-type transistor is positioned adjacent to the non-volatile memory transistor, the second voltage-type transistor is positioned adjacent to the first voltage-type transistor, and the third voltage-type transistor is positioned adjacent to the second voltage-type transistor, wherein the first voltage type transistor is positioned between the second voltage type transistor and the non-volatile memory transistor, and wherein the second voltage-type transistor is positioned between the third voltage-type transistor and the first voltage-type transistor.

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29. (amended) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

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a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate;

wherein the first voltage-type transistor operates at a lower voltage range than that of the second voltage-type transistor, and the second voltage-type transistor operates at a lower voltage range than that of the third voltage-type transistor; and

wherein the first voltage-type transistor is positioned adjacent to the non-volatile memory transistor, the second voltage-type transistor is positioned adjacent to the first voltage-type transistor, and the third voltage-type transistor is positioned adjacent to the second voltage-type transistor, wherein the first voltage type transistor is positioned between the second voltage type